

ABSTRACT

A semiconductor memory device comprises a memory array in which memory cells having variable resistive elements (R_{11} to R_{ij}) whose electrical resistance is varied by electrical stress and is held even after the electrical stress is released and selection transistors (T_{11} to T_{ij}) comprising N type MOSFETs are arranged with a matrix; programming means for applying the electrical stress to the variable resistive elements (R_{11} to R_{ij}) to program data into the memory cell; programming state detection means for detecting the variation in the electrical resistance at the time of the programming operation; and programming control means for stopping the application of the electrical stress when the electrical resistance is varied to a predetermined reference value. With this structure, it is possible to constitute the semiconductor memory device in which the time required for programming data is shortened and the programming precision is high.

Reference Drawing: Fig. 1